RECEIVED
CENTRAL FAX CENTER
OCT 15 2007

A-75000

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

CHIOU-FENG CHEN ET AL.

Serial No. 10/753,103

Filed: January 6, 2004

For: NAND FLASH MEMORY WITH ENHANCED PROGRAM AND ERASE PERFORMANCE, AND FABRICATION PROCESS

Examiner: Johannes P. Mondt

Group Art Unit: 2826

Confirmation No. 2773

October 15, 2007

TRANSMITTAL OF APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith is applicant's Brief on Appeal in this matter.

The filing fee for the brief has already been paid in an earlier appeal. However, the Commissioner is authorized to charge any additional fees which may be required, including extension fees, and to credit any overpayments to Deposit Account 50-2975, Order No. A-75000.

Respectfully submitted,

Edward S. Wright
Reg. No. 24,903

CERTIFICATE OF FACSIMILE TRANSMISSION

THIS CORRESPONDENCE AND THE ACCOMPANYING BRIEF ARE BEING FORWARDED TO THE PATENT OFFICE FOR FILING VIA FACSIMILE TRANSMISSION TO (571) 273-8300 ON OCTOBER 15, 2007.

EDWARD S. WRIGHT

RECEIVED
CENTRAL FAX CENTER
OCT 15 2007

A-75000

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

CHIOU-FENG CHEN ET AL.

Serial No. 10/753,103

Filed: January 6, 2004

For: NAND FLASH MEMORY WITH ENHANCED PROGRAM AND ERASE PERFORMANCE, AND FABRICATION PROCESS

Examiner: Johannes P. Mondt

Group Art Unit: 2826

Confirmation No. 2773

October 15, 2007

BRIEF ON APPEAL

Edward S. Wright
1100 Alma Street, Suite 207
Menlo Park, CA 94025
(650) 330-0830 (Telephone)
(650) 330-0831 (Facsimile)

RECEIVED
CENTRAL FAX CENTER
OCT 15 2007

Table of Contents

PAGE 3/20 * RCVD AT 10/15/2007 7:45:47 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-2/15 * DNIS:2738300 * CSID:650 330 0831 * DURATION (mm-ss):06-50

RECEIVED
CENTRAL FAX CENTER
OCT 15 2007

REAL PARTY IN INTEREST

The real party in interest is Silicon Storage Technology, Inc., a California corporation with a place of business in Sunnyvale, California, to whom the application has been assigned.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAIMS

The application was filed originally with Claims 1 - 23. In an amendment filed October 27, 2005, Claims 14 and 23 were cancelled to minimize filing fees since they had been withdrawn from consideration, Claims 1 - 2, 4 - 6, 8 - 12, 15 - 16, 18 - 20 and 22 were amended, and Claim 24 was added. In an amendment filed May 23, 2007, Claims 3, 9, 10, 11, 17 and 21 were amended. Claims 1 - 13, 15 - 22 and 24 are on appeal. Currently, no claims stand allowed.

STATUS OF AMENDMENTS

The only amendment filed since the action from which this appeal is taken is one filed August 7, 2007 in which only the Abstract was amended.

SUMMARY OF CLAIMED SUBJECT MATTER

The claims on appeal are directed to a NAND flash memory cell array which, as defined by Claim 1, illustrated in Figures 2 and 7 and described at Page 5, line 6 to Page 6, line 27 and Page 12, lines 1 - 14, comprises a substrate (41) having an active area (52), a bit line diffusion (50) and a source region (51) in the active area with no other diffusions in the active area between the bit line diffusion (50) and the source region (51), a plurality of stacked gates (36) and select gates (43 - 45) arranged alternately in a row above the active area between the bit line diffusion (50) and the source region (51), with each of the stacked gates (36) having a control gate (36) positioned above a floating gate (37) and the last select gate (45) in the row at least partially overlapping the source region (51), a bit line (57) above the row, and a bit line contact (46) interconnecting the bit line (57) and the bit line diffusion (50).

Claims 2 - 13 depend from Claim 1. Claim 2 further specifies that the stacked gates (36) and the select gates (43 - 45) are self-aligned relative to each other.

Claim 3 further calls for a tunnel oxide (40) between the floating gates (37) and the substrate (41, 52), a first dielectric (47) between the floating gates (37) and the select gates (43 - 45), and a second dielectric (42) between the floating gates (37) and the control gates (38), with the tunnel oxide being thinner than the first and second dielectrics.

Claim 4 further specifies that the control gates (38) and the select gates (43 - 45) surround the floating gates (37) in a manner which provides inter-gate capacitances between the select gates (43 - 45) and the floating gates (37) and between the control gates (38)

and the floating gates (37) which are large enough to couple voltages between the select gates (43 - 45) and the floating gates (37) and between the control gates (38) and the floating gates (37). See Page 9, lines 8 - 15.

Claim 5 further specifies that erase paths extend from the floating gates (37), through tunnel oxides (40) below the floating gates (37) to channel regions in the substrate (41, 52), and voltage is coupled to the floating gates (37) both from the control gates (38) and from the select gates (43 - 45). See Page 9, line 1 to Page 10, line 2.

Claim 6 specifies that program paths extend from off-gate channel regions between the select gates (43 - 45) and the floating gates (37) to the floating gates (37), and voltage is coupled to the floating gates (37) both from the control gates (38) and from the select gates (43, 45) on the sides of the stacked gates (36) toward the source region (51).

Claim 7 specifies that program paths extend from off-gate channel regions between the select gates (43 - 45) and the floating gates (37) to the floating gates (37), and the select gate (43, 44) on the bit line side of the stacked gates (36) in a selected cell is biased at a lower voltage than the other select gates (43, 45) in the row to control channel current for efficient hot carrier injection during a program operation. See Page 10, lines 8 - 30.

Claim 8 specifies that the select gates (43 - 45) in unselected cells are biased at a voltage to turn on the channels beneath them to form a conduction path between the bit line diffusion and the source region. See Fig. 6.

Claim 9 specifies that the bit line (57) for a row containing a selected cell to be programmed is held at 0 volts, a first positive voltage is applied to a cell select gate (43 - 45) for the selected cell, a voltage higher than the first positive voltage is applied to the source region (51) at the end of the row in which the selected cell is located, a relatively high positive voltage is applied to the control gate (38) in the selected cell, a voltage higher than the first positive voltage is applied to the select gates (43 - 45) for unselected cells, and a voltage higher than the first positive voltage is applied to the control gates (38) in the unselected cells. See Page 10, lines 8 - 17.

Claim 10 specifies that an erase path is formed by a first negative voltage on the control gates (38) and a negative voltage smaller than the first negative voltage on the select gates (43 - 45), with the bit line diffusion (50), the source region (51) and the P-well (52) at 0 volts. See Page 9, lines 16 - 20.

Claim 11 wherein an erase path is formed by a first negative voltage on the control gates (38) and a negative voltage smaller than the first negative voltage on the select gates (43 - 45), with the active area (52) at a positive voltage and the bit line diffusion (50) and the source region (51) floating. See Page 9, lines 20 - 23.

Claim 12 specifies that a read path is formed by turning on the select transistors (43 - 45) and the stacked control and floating gate transistors (38, 37) in unselected cells, with

PAGE 5/20 * RCVD AT 10/15/2007 7:45:47 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-2/15 * DNIS:2738300 * CSID:650 330 0831 * DURATION (mm-ss):06-50

the common source (51) at 0 volts, the bit line diffusion (50) at 1 - 3 volts, and the control gate (38) of the selected cell biased at 0 – 1.5 volts to form a conduction channel under the floating gate (37) for an erase state and a non-conduction channel for a program state. See Fig. 6 and Page 11, lines 18 - 30.

Claim 13 further calls for an erase path which can erase the whole cell array simultaneously and a program path which is single cell selectable. See Page 17, lines 27 - 29.

As defined by Claim 15, illustrated in Figure 7 and described at Page 12, lines 1 - 14, the NAND flash memory cell array comprises a substrate (41) having an active area (52), a bit line diffusion (50) and a source diffusion (51) in the active area with no other diffusions in the active area (52) between the bit line diffusion and the source diffusion, a plurality of stacked gates (36) and select gates (43 - 45) arranged alternately in a row above the active area (52) between the bit line diffusion (50) and the source diffusion (51), with each of the stacked gates (36) having a control gate (38) positioned above a floating gate (37) and the last select gate (45) in the row being directly above the source diffusion (51), a bit line (57) above the row, and a bit line contact (46) interconnecting the bit line (57) and the bit line diffusion (50).

Claims 16 - 18 depend from Claim 15. Claim 16 further specifies that the select gates (43 - 45) are self-aligned to the control and floating gates (38, 37). Claim 17 calls for a tunnel oxide (40) between the floating gates (37) and the substrate (41, 52), a first dielectric (47) between the floating gates (37) and the select gates (43 - 45), and a second dielectric (42) between floating gates (37) and control gates (38), with the tunnel oxide being thinner than the first and second dielectrics. Claim 18 specifies that the control gates (38) and the select gates (43 - 45) surround the floating gates (37) in a manner which provides inter-gate capacitances between the select gates (43 - 45) and the floating gates (37) and between the control gates (38) and the floating gates (37) which are large enough to couple voltages between the select gates (43 - 45) and the floating gates (37) and between the control gates (38) and the floating gates (37). See Page 9, lines 8 - 15.

As defined by Claim 19, illustrated in Figures 2, 4, 7 and 8 and described at Page 5, line 6 to Page 6, line 27 and Page 12, lines 1 - 14, the NAND flash memory cell array comprises a substrate (41) having an active area (42), bit line diffusions (50) and source diffusions (51) spaced alternately in the active area (52) with no other diffusions between them, a plurality of stacked gates (36) and select gates (43 - 45) arranged alternately in rows between the bit line diffusions (50) and the source diffusions (51), with each of the stacked gates (36) having a control gate (38) positioned above a floating gate (37) and the last select gates (45) in each of the rows at least partially overlapping the source diffusions (51) between

PAGE 6/20 * RCVD AT 10/15/2007 7:45:47 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-2/15 * DNIS:2738300 * CSID:650 330 0831 * DURATION (mm-ss):06-50

the rows, a bit line (57) above each row, and bit line contacts (46) interconnecting the bit lines (57) and the bit line diffusions (50).

Claims 20 - 22 depend from Claim 19. Claim 20 further specifies that the select gates (43 - 45) are self-aligned to the control and floating gates (38, 37). Claim 21 calls for a tunnel oxide (40) between the floating gates (37) and the substrate (41, 52), a first dielectric (47) between the floating gates (37) and the select gates (43 - 45), and a second dielectric (42) between floating gates (37) and control gates (38), with the tunnel oxide being thinner than the first and second dielectrics. Claim 22 specifies that the control gates (38) and the select gates (43 - 45) surround the floating gates (37) in a manner which provides inter-gate capacitances between the select gates (43 - 45) and the floating gates (37) and between the control gates (38) and the floating gates (37) which are large enough to couple voltages between the select gates (43 - 45) and the floating gates (37) and between the control gates (38) and the floating gates (37). See Page 9, lines 8 - 15.

As defined by Claim 24, illustrated in Figures 2 and 7 and described at Page 5, line 6 to Page 6, line 27 and Page 12, lines 1 - 14, the NAND flash memory cell array comprises a substrate (41) having an active area (52), a bit line diffusion (50) and a source region (51) in the active area (52) with no other diffusions in the active area between the bit line diffusion (50) and the source region (51), a plurality of stacked gates (36) and select gates (43) arranged alternately in a row above the active area (52) between the bit line diffusion (50) and the source region (51), with each of the stacked gates (36) having a control gate (38) and a floating gate (37) with self-aligned sides adjacent to the select gates (43 - 45), erase paths between the floating gates (37) and channel regions in the active area beneath the stacked gates (36), and voltage coupling from the control gates (38) and the select gates (43 - 45) to the floating gates (37). See Page 9, lines 8 - 12.

GROUNDS OF REJECTION

All of the claims currently pending in the application (Claims 1 - 13, 15 - 22 and 24) have been rejected under 35 U.S. C. §103 as being unpatentable over Hsu et al. (U.S. 6,911,690) in view of either prior art allegedly admitted by applicant in combination with Chapman et al. (U.S. 6,118,161) or Sakui et al. (U.S. 6,411,548) in combination with Chapman et al.

ARGUMENT

In making the rejection, the Examiner has misconstrued and mischaracterized what is actually found in the references and has tried to combine selected elements from the different references when there is no basis for doing so.

The array shown in Hsu et al. has a string of memory cell structures 132a - 132d formed between drain and source regions 124, 126. There are no bit lines, bit line diffusions

PAGE 7/20 * RCVD AT 10/15/2007 7:45:47 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-2/15 * DNIS:2738300 * CSID:650 330 0831 * DURATION (mm-ss):06-50

or bit line contacts, as in applicant's invention, nor is there any overlapping or partial overlapping of a source region by a select gate. In that regard, it will be noted that the paragraph bridging Columns 5 and 6 of Hsu et al. makes it quite clear that region 124 is a drain region and not a bit line diffusion. When challenged to provide any support he may have for characterizing drain region 124 as a bit line diffusion, The Examiner has failed to do so.

In attempting to create a bit line diffusion where none exists, the Examiner also makes the illogical, unsupported and totally specious argument that a bit line diffusion inherently is contacted with a bit line and that both a bit line and a bit line contact must therefore exist. Notwithstanding the Examiner's efforts, the simple fact is that there are no bit line diffusions, no bit lines and no bit line contacts in Hsu et al.

Moreover, notwithstanding the Examiner's arguments about the inherency of bit lines, bit line contacts and bit line diffusions, nowhere in the prior art is there any suggestion of bit line and source diffusions at opposite ends of a row of alternating stacked gates and select gates with no other diffusions in the active area between the bit line diffusion and the source region. Even if such elements were inherent in the device of Hsu et al., where would they be? Would the Examiner change the source region or the drain region of Hsu et al. to a bit line diffusion and then add a bit and a bit line contact? If so, where is the motivation for doing so, and how does the Examiner know that the resulting device would work?

Sakui et al. and Figure 1 of applicant's disclosure are cited as showing a select gate partially overlapping a source region, a feature the Examiner acknowledges is not found in Hsu et al. However, neither Sakui et al. nor the prior art discussed in the background section of applicant's disclosure even remotely suggests a select gate which partially overlaps a source region in a memory cell array having the other elements of applicant's invention. There is no motivation or other basis for combining the teachings of either Sakui et al. or the background section of applicant's disclosure with those of Hsu et al., and there is likewise no suggestion as to how it might be done or what useful purpose it might serve. Moreover, the structure shown in Hsu et al. does not lend itself to having a select gate partially overlapping source region 126 because there is no select gate at that end of the string of cells. Hence, adding a select gate and then having it partially overlap the source region is far beyond the teachings of the references.

Chapman et al. is cited as showing that for low series resistance and consistent high performance, it is well known that a gate should overlap with a source. However, that statement was made in the specific context of a MOSFET, not a NAND flash memory cell array, and there is no basis for the Examiner's contention that the select gate in any NAND flash memory device is no different from an ordinary gate in any transistor.

PAGE 8/20 * RCVD AT 10/15/2007 7:45:47 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-2/15 * DNIS:2738300 * CSID:650 330 0831 * DURATION (mm-ss):06-50

Claims 1 - 13

Claim 1 distinguishes over the combined teachings of the references in calling for a bit line diffusion and a source region in the active area of a substrate with no other diffusions in the active area between the bit line diffusion and the source region, a plurality of stacked gates and select gates arranged alternately in a row above the active area between the bit line diffusion and the source region, with each of the stacked gates having a control gate positioned above a floating gate and the last select gate in the row at least partially overlapping the source region, a bit line above the row, and a bit line contact interconnecting the bit line and the bit line diffusion. As discussed above, the references fail to teach or even suggest a bit line diffusion and a source region in the active area of a substrate with no other diffusions in the active area between the bit line diffusion and the source region. They likewise fail to show or suggest a row of stacked gates and select gates with the last select gate in the row at least partially overlapping the source region, and they further fail to show a bit line above the row and a bit line contact interconnecting the bit line and the bit line diffusion.

Claims 2 - 13 depend from Claim 1 and distinguish over the references for the same reasons as their parent claim. In addition, they call for additional features which are not found in or suggested by the references.

Claim 2 specifies that the stacked gates and the select gates are self-aligned relative to each other. In rejecting this claim, the Examiner first proclaims that "stacked gates and select gates are aligned to each other" and then tries to dismiss self-alignment as being a process limitation. He is wrong on both counts. There is no support whatsoever for the statement that stacked gates and select gates are aligned to each other. That statement was made without reference to any particular structure and is meaningless. Moreover, it is not what the claim calls for, and while having the stacked gates and the select gates self-aligned with each other may be the result of the manner in which the gates are formed, it is nevertheless a structural limitation.

Claim 3 further distinguishes in calling for a tunnel oxide between the floating gates and the substrate, a first dielectric between the floating gates and the select gates, and a second dielectric between the floating gates and the control gates, with the tunnel oxide being thinner than the first dielectric and the second dielectric. As the Examiner has acknowledged, this relationship is not taught by Hsu et al. or the other references. Hsu et al. is silent as to the relative thickness of the different dielectrics, and there is no basis for the Examiner's argument that quantum mechanics and cost considerations mandate that two of the dielectric layers should be thicker than the other.

Claim 4 further distinguishes in specifying that the control gates and the select gates surround the floating gates in a manner which provides inter-gate capacitances between

PAGE 9/20 * RCVD AT 10/15/2007 7:45:47 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-2/15 * DNIS:2738300 * CSID:650 330 0831 * DURATION (mm-ss):06-50

the select gates and the floating gates and between the control gates and the floating gates which are large enough to couple voltages between the select gates and the floating gates and between the control gates and the floating gates. In arguing that any non-zero inter-gate capacitance implies a voltage coupling between the gates, the Examiner has failed to consider the clear language of the claim which defines the control gates and the select gates as surrounding the floating gates.

Claim 5 further specifies that erase paths extend from the floating gates, through tunnel oxides below the floating gates to channel regions in the substrate, and voltage is coupled to the floating gates both from the control gates and from the select gates. Although the Examiner states that voltage is coupled to the floating gates both from the control gates and from the select gates in Hsu et al., he offers no support for that statement, and the argument about the tunnel oxide not reducing the voltage on the floating gate from the voltage in the channel is irrelevant and specious.

Claim 6 specifies that program paths extend from off-gate channel regions between the select gates and the floating gates to the floating gates, and voltage is coupled to the floating gates both from the control gates and from the select gates on the sides of the stacked gates toward the source region. In rejecting this claim, the Examiner makes the unsupported argument that programming paths are allowed to exist because the off-gate channel regions are conductive through the action of the gates, and he once again makes the irrelevant and specious argument about the the claimed paths are found in Hsu et al. because the tunnel oxide not reducing the voltage on the floating gate from the voltage in the channel.

Claims 7 - 12 further distinguish over the references in calling for the application of specific voltages to different elements in the memory array.

In that regard, Claim 7 specifies that program paths extend from off-gate channel regions between the select gates and the floating gates to the floating gates, and the select gate on the bit line side of the stacked gates in a selected cell is biased at a lower voltage than the other select gates in the row to control channel current for efficient hot carrier injection during a program operation. In rejecting this claim, the Examiner makes the same erroneous argument about the program paths that he made in connection with Claim 6, then he tries to ignore the remainder of the claim on the basis that it is functional or intended use. The language in question specifies that the select gate on the bit line side of the stacked gates in a selected cell is biased at a lower voltage than the other select gates in the row to control channel current for efficient hot carrier injection during a program operation. Contrary to the Examiner's contention, the biasing of a specific element in a specific manner relative to other specific elements in a specific operational mode is indeed a structural limitation.

PAGE 10/20 * RCVD AT 10/15/2007 7:45:47 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-2/15 * DNIS:2738300 * CSID:650 330 0831 * DURATION (mm-ss):06-50

Claim 8 specifies that the select gates in unselected cells are biased at a voltage to turn on the channels beneath them to form a conduction path between the bit line diffusion and the source region. Here again, the Examiner has erred in ignoring a specific structural limitation as to the manner in which specific elements are biased, and the intended use or functional language argument is the same one he made in rejecting Claim 7.

Claim 9 specifies that the bit line for a row containing a selected cell to be programmed is held at 0 volts, a first positive voltage is applied to a cell select gate for the selected cell, a voltage higher than the first positive voltage is applied to the source region at the end of the row in which the selected cell is located, a voltage higher than the first positive voltage is applied to the control gate in the selected cell, a voltage higher than the first positive voltage is applied to the select gates for unselected cells, and a voltage higher than the first positive voltage is applied to the control gates in the unselected cells. Once again, the Examiner has failed to give patentable weight to the specific limitations which distinguish over the references, and the intended use or functional language argument is the same one he made in rejecting the other claims.

Claim 10 specifies that an erase path is formed by a first negative voltage on the control gates and a negative voltage smaller than the first negative voltage on the select gates, with the bit line diffusion, the source region and the P-well at 0 volts. Here again, the Examiner has failed to give patentable weight to the specific limitations which distinguish over the references, and the intended use or functional language argument is the same one he made in rejecting the other claims.

Claim 11 specifies that an erase path is formed by a first negative voltage on the control gates and negative voltage smaller than the first negative voltage on the select gates, with the active area at a positive voltage and the bit line diffusion and the source region floating. Once again, the Examiner has failed to give patentable weight to the specific limitations which distinguish over the references, and the intended use or functional language argument is the same one he made in rejecting the other claims.

Claim 12 specifies that a read path is formed by turning on the select transistors and the stacked control and floating gate transistors in unselected cells, with the common source at 0 volts, the bit line diffusion at 1 - 3 volts, and the control gate of the selected cell biased at 0 – 1.5 volts to form a conduction channel under the floating gate for an erase state and a non-conduction channel for a program state. Here again, the Examiner has failed to give patentable weight to the specific limitations which distinguish over the references, and the intended use or functional language argument is the same one he made in rejecting the other claims.

In rejecting Claims 7 - 12, the Examiner has taken the position that biasing and the application of other voltages are "intended use" or functional limitations to which no

PAGE 11/20 * RCVD AT 10/15/2007 7:45:47 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-2/15 * DNIS:2738300 * CSID:650 330 0831 * DURATION (mm-ss):06-50

patentable weight is given. In so doing, he has overlooked the fact that the biasing of a specific element in a specific manner relative to other specific elements in a specific operational mode and the application of specific and/or relative voltages to specific elements are indeed structural limitations. Although they may define the structure as it is in use, they are nevertheless structural in nature and, therefore, entitled to patentable weight.

Claim 13 further calls for an erase path which can erase the whole cell array simultaneously and a program path which is single cell selectable. Rather than pointing to any specific structure or teaching in the references, the Examiner simply argues that an erase path *"can"* be formed by biasing of control gates and select gates and that such biasing *"can"* be done for every cell in the array in order to erase the whole array simultaneously. He makes a similar, unsupported argument that a program path which is single cell selectable *"can"* be created through appropriate biasing. Such conjecture on the part of the is clearly not a proper basis for rejection under 35 U.S.C. §103, and he cannot use the intended use or functional language argument to ignore specific structural limitations which distinguish over the references.

Claims 15 - 18

Claim 15 distinguishes over the references in calling for a bit line diffusion and a source diffusion in the active area of a substrate with no other diffusions in the active area between the bit line diffusion and the source diffusion, a plurality of stacked gates and select gates arranged alternately in a row above the active area between the bit line diffusion and the source diffusion, with each of the stacked gates having a control gate positioned above a floating gate and the last select gate in the row being directly above the source diffusion, a bit line above the row, and a bit line contact interconnecting the bit line and the bit line diffusion. As noted above, the references fail to teach or even suggest a bit line diffusion and a source region in the active area of a substrate with no other diffusions in the active area between the bit line diffusion and the source region. They likewise fail to show or suggest a row of stacked gates and select gates with the last select gate in the row being directly above the source region, and the Examiner is mistaken in suggesting that this structure is shown in Sakui et al. They also fail to show a bit line above the row, and a bit line contact interconnecting the bit line and the bit line diffusion.

Claims 16 - 18 depend from Claim 15 and distinguish over the references for the same reasons as their parent claim. In addition, they call for additional features which are not found in or suggested by the references.

Claim 16 specifies that the select gates are self-aligned to the control and floating gates. In rejecting this claim, the Examiner has made substantially the same specious arguments he made in rejecting Claim 2. The claim is directed to a specific structural feature that is not found in or suggested by the references.

PAGE 12/20 * RCVD AT 10/15/2007 7:45:47 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-2/15 * DNIS:2738300 * CSID:650 330 0831 * DURATION (mm-ss):06-50

Claim 17, like Claim 3, further distinguishes in calling for a tunnel oxide between the floating gates and the substrate, a first dielectric between the floating gates and the select gates, and a second dielectric between the floating gates and the control gates, with the tunnel oxide being thinner than the first and second dielectrics. As discussed above, this relationship is not taught by Hsu et al. or the other references, Hsu et al. is silent as to the relative thickness of the different dielectrics, and there is no basis for the Examiner's argument that quantum theory and cost considerations mandate that two of the dielectric layers should be thicker than the other.

Claim 18, like Claim 4, further distinguishes in specifying that the control gates and the select gates surround the floating gates in a manner which provides inter-gate capacitances between the select gates and the floating gates and between the control gates and the floating gates which are large enough to couple voltages between the select gates and the floating gates and between the control gates and the floating gates. In arguing that any non-zero inter-gate capacitance implies a voltage coupling between the gates, the Examiner has once again failed to consider the clear language of the claim which defines the control gates and the select gates as surrounding the floating gates.

Claims 19 - 22

Claim 19 distinguishes over the references in calling for a substrate having an active area, bit line diffusions and source diffusions spaced alternately in the active area with no other diffusions between them, a plurality of stacked gates and select gates arranged alternately in rows between the bit line diffusions and the source diffusions, with each of the stacked gates having a control gate positioned above a floating gate and the last select gates in each of the rows at least partially overlapping the source diffusions between the rows, a bit line above each row, and bit line contacts interconnecting the bit lines and the bit line diffusions. As discussed above, the references taken individually or collectively fail to disclose or even remotely suggest a memory cell array having these features.

Claims 20 - 22 depend from Claim 21 and are directed to patentable subject matter for the same reasons as their parent claim. In addition, they call for additional features which are not found in or suggested by the references.

Claim 20 specifies that the floating gate and the control gate in each of the stacked gates are self-aligned with respect to each other. In rejecting this claim, the Examiner has once again made the same specious arguments he made in rejecting Claim 2. The claim is directed to a specific structural feature that is not found in or suggested by the references.

Claim 21, like Claim 3 and Claim 17, further distinguishes in calling for a tunnel oxide between the floating gates and the substrate, a first dielectric between the floating gates and the select gates, and a second dielectric between the floating gates and the control gates, with the tunnel oxide being thinner than the first and second dielectrics.

PAGE 13/20 * RCVD AT 10/15/2007 7:45:47 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-2/15 * DNIS:2738300 * CSID:650 330 0831 * DURATION (mm-ss):06-50

As discussed above and acknowledged by the Examiner, this relationship is not taught by Hsu et al. or the other references, Hsu et al. is silent as to the relative thickness of the different dielectrics, and there is no basis for the Examiner's argument that quantum theory and cost considerations mandate that two of the dielectric layers should be thicker than the other.

Claim 22, like Claim 4 and Claim 17, further distinguishes in specifying that the control gates and the select gates surround the floating gates in a manner which provides inter-gate capacitances between the select gates and the floating gates and between the control gates and the floating gates which are large enough to couple voltages between the select gates and the floating gates and between the control gates and the floating gates. . In arguing that any non-zero inter-gate capacitance implies a voltage coupling between the gates, the Examiner has once again failed to consider the clear language of the claim which defines the control gates and the select gates as surrounding the floating gates.

Claim 24

Claim 24 distinguishes over the references in calling for a bit line diffusion and a source region in the active area of a substrate with no other diffusions in the active area between the bit line diffusion and the source region, a plurality of stacked gates and select gates arranged alternately in a row above the active area between the bit line diffusion and the source region, with each of the stacked gates having a control gate and a floating gate with self-aligned sides adjacent to the select gates, erase paths between the floating gates and channel regions in the active area beneath the stacked gates, and voltage coupling from the control gates and the select gates to the floating gates.

As discussed above, Hsu et al. and the other references fail to teach or suggest a bit line diffusion and a source region in the active area of a substrate with no other diffusions in the active area between the bit line diffusion and the source region, stacked gates having a control gate and a floating gate with self-aligned sides adjacent to select gates, and voltage coupling from the control gates and the select gates to the floating gates. There is no bit line in Hsu et al. and, *a fortiori*, no other diffusions between a bit line and a source region.

In rejecting Claim 24, the Examiner characterizes the control gates and floating gates in Hsu et al. as having "aligned sides" adjacent to the select gates and then argues that the difference between "aligned" and "self-aligned" constitutes a product-by-process limitation and is non-limiting. However, as discussed above, even though the self-alignment is the result of the process by which the sides of the gates are formed, it is nevertheless a structural feature that cannot be ignored.

With regard to the voltage coupling from the control gates and the select gates to the floating gates, the Examiner makes the unsupported and specious argument that such

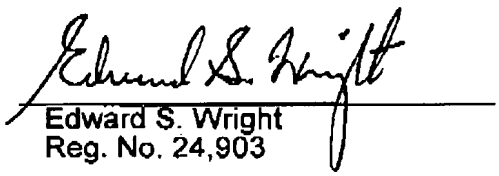
PAGE 14/20 * RCVD AT 10/15/2007 7:45:47 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-2/15 * DNIS:2738300 * CSID:650 330 0831 * DURATION (mm-ss):06-50

coupling is inherent because the control gates control the voltage of the floating gates and the select gates determine whether or not there is a channel in which charge carriers can approach the floating gates. As resourceful as it may be, that is not what the claim calls for.

SUMMARY AND CONCLUSION

It is respectfully submitted that the rejections which the Examiner has made cannot be sustained and that the action of the Examiner should be reversed.

Respectfully submitted,



Edward S. Wright
Reg. No. 24,903

Law Offices of Edward S. Wright
1100 Alma Street, Suite 207
Menlo Park, CA 94025
(650) 330-0830 (Telephone)
(650) 330-0831 (Facsimile)
twright@claim1.com

PAGE 15/20 * RCVD AT 10/15/2007 7:45:47 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-2/15 * DNIS:2738300 * CSID:650 330 0831 * DURATION (mm-ss):06-50

CLAIMS APPENDIX

The Claims on Appeal

1. A NAND flash memory cell array, comprising: a substrate having an active area, a bit line diffusion and a source region in the active area with no other diffusions in the active area between the bit line diffusion and the source region, a plurality of stacked gates and select gates arranged alternately in a row above the active area between the bit line diffusion and the source region, with each of the stacked gates having a control gate positioned above a floating gate and the last select gate in the row at least partially overlapping the source region, a bit line above the row, and a bit line contact interconnecting the bit line and the bit line diffusion.

2. The memory cell array of Claim 1 wherein the stacked gates and the select gates are self-aligned relative to each other.

3. The memory cell array of Claim 1 including a tunnel oxide between the floating gates and the substrate, a first dielectric between the floating gates and the select gates, and a second dielectric between the floating gates and the control gates, with the tunnel oxide being thinner than the first and second dielectrics.

4. The memory cell array of Claim 1 wherein the control gates and the select gates surround the floating gates in a manner which provides inter-gate capacitances between the select gates and the floating gates and between the control gates and the floating gates which are large enough to couple voltages between the select gates and the floating gates and between the control gates and the floating gates.

5. The memory cell array of Claim 1 wherein erase paths extend from the floating gates, through tunnel oxides below the floating gates to channel regions in the substrate, and voltage is coupled to the floating gates both from the control gates and from the select gates.

6. The memory cell array of Claim 1 wherein program paths extend from off-gate channel regions between the select gates and the floating gates to the floating gates, and voltage is coupled to the floating gates both from the control gates and from the select gates on the sides of the stacked gates toward the source region.

7. The memory cell array of Claim 1 wherein program paths extend from off-gate channel regions between the select gates and the floating gates to the floating gates, and the select gate on the bit line side of the stacked gates in a selected cell is biased at a lower voltage than the other select gates in the row to control channel current for efficient hot carrier injection during a program operation.

8. The memory cell array of Claim 1 wherein the select gates in unselected cells are biased at a voltage to turn on the channels beneath them to form a conduction path between the bit line diffusion and the source region.

9. The memory cell array of Claim 1 wherein the bit line for a row containing a selected cell to be programmed is held at 0 volts, a first positive voltage is applied to a cell select gate for the selected cell, a voltage higher than the first positive voltage is applied to the source region at the end of the row in which the selected cell is located, a voltage higher than the first positive voltage is applied to the control gate in the selected cell, a voltage higher than the first positive voltage is applied to the select gates for unselected cells, and a voltage higher than the first positive voltage is applied to the control gates in the unselected cells.

10. The memory cell array of Claim 1 wherein an erase path is formed by a first negative voltage on the control gates and a negative voltage smaller than the first negative voltage on the select gates, with the bit line diffusion, the source region and the P-well at 0 volts.

11. The memory cell array of Claim 1 wherein an erase path is formed by a first negative voltage on the control gates and a negative voltage smaller than the first negative voltage on the select gates, with the active area at a positive voltage and the bit line diffusion and the source region floating.

12. The memory cell array of Claim 1 wherein a read path is formed by turning on the select transistors and the stacked control and floating gate transistors in unselected cells, with the common source at 0 volts, the bit line diffusion at 1 - 3 volts, and the control gate of the selected cell biased at 0 – 1.5 volts to form a conduction channel under the floating gate for an erase state and a non-conduction channel for a program state.

13. The memory cell array of Claim 1 including an erase path which can erase the whole cell array simultaneously and a program path which is single cell selectable.

15. A NAND flash memory cell array, comprising: a substrate having an active area, a bit line diffusion and a source diffusion in the active area with no other diffusions in the active area between the bit line diffusion and the source diffusion, a plurality of stacked gates and select gates arranged alternately in a row above the active area between the bit line diffusion and the source diffusion, with each of the stacked gates having a control gate positioned above a floating gate and the last select gate in the row being directly above the source diffusion, a bit line above the row, and a bit line contact interconnecting the bit line and the bit line diffusion.

16. The memory cell array of Claim 15 wherein the select gates are self-aligned to the control and floating gates.

17. The memory cell array of Claim 15 including a tunnel oxide between the floating gates and the substrate, a first dielectric between the floating gates and the select gates, and a second dielectric between floating gates and control gates, with the tunnel oxide being thinner than the first and second dielectrics.

18. The memory cell array of Claim 15 wherein the control gates and the select gates surround the floating gates in a manner which provides inter-gate capacitances between the select gates and the floating gates and between the control gates and the floating gates which are large enough to couple voltages between the select gates and the floating gates and between the control gates and the floating gates.

19. A NAND flash memory cell array, comprising: a substrate having an active area, bit line diffusions and source diffusions spaced alternately in the active area with no other diffusions between them, a plurality of stacked gates and select gates arranged alternately in rows between the bit line diffusions and the source diffusions, with each of the stacked gates having a control gate positioned above a floating gate and the last select gates in each of the rows at least partially overlapping the source diffusions between the rows, a bit line above each row, and bit line contacts interconnecting the bit lines and the bit line diffusions.

20. The memory cell array of Claim 19 wherein the floating gate and the control gate in each of the stacked gates are self-aligned with respect to each other.

21. The memory cell array of Claim 19 including a tunnel oxide between the floating gates and the substrate, a first dielectric between the floating gates and the select gates, and a second dielectric between floating gates and control gates, with the tunnel oxide being thinner than the first and second dielectrics.

22. The memory cell array of Claim 19 wherein the control gates and the select gates surround the floating gates in a manner which provides inter-gate capacitances between the select gates and the floating gates and between the control gates and the floating gates which are large enough to couple voltages between the select gates and the floating gates and between the control gates and the floating gates.

24. A NAND flash memory cell array, comprising: a substrate having an active area, a bit line diffusion and a source region in the active area with no other diffusions in the active area between the bit line diffusion and the source region, a plurality of stacked gates and select gates arranged alternately in a row above the active area between the bit line diffusion and the source region, with each of the stacked gates having a control gate and a floating gate with self-aligned sides adjacent to the select gates, erase paths between the floating gates and channel regions in the active area beneath the stacked gates, and voltage coupling from the control gates and the select gates to the floating gates.

RECEIVED
CENTRAL FAX CENTER
OCT 15 2007

EVIDENCE APPENDIX

Copies of Evidence Submitted

None

DECISIONS APPENDIX

Copies of Decisions in Related Appeals and Interferences

None